IN THE CLAIMS:

1-32 canceled

33. (new) A method for the production of semiconductor layer structures, comprising at least one strain-compensating layer for surrounding layer(s) of a semiconductor device, whereby the strain-compensating layer(s) are semiconductor-layers strained by tensile stress and wherein the layer succession features one or several layers with arsenic and/or phosphorus by use of TBAs sources and/or TBP sources, wherein the strain compensating layer(s) are achieved and compressively or tensilely strained by MOVPE at a temperature in the range of 300°C to 590°C by use of tertiarybutylarsine (t-C4H9AsH2) and tertiarybutylphosphine (t-C4H9PH2, TBP).

34. (new) Method according to claim 33 wherein the strain-compensating layers are deposited within the layers to be compensated in their individual or common strain.

35. (new) Method according to claim 33 wherein an aluminum-containing AlGaAs/AlAs slight compressive strain can be tensilely compensated due to low concentrations of phosphorus.

36. (new) Method according to claim 33 wherein compression-strained semiconductor layers are compensated for their strain.